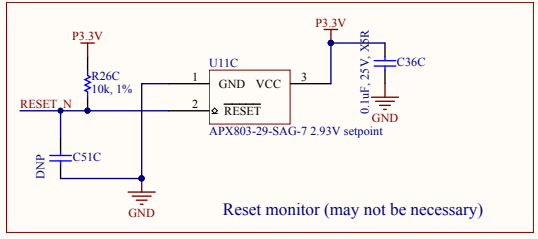
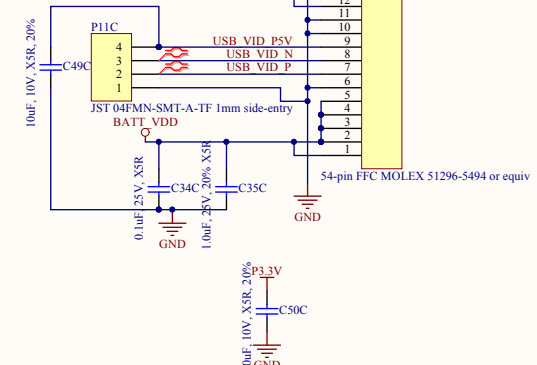


0.5A / contact
 4x for LCD digital logic (2A max)
 5x for BL (2.5A x Vbat watts)

| Pin | Signal |
|-----|---------------|
| 54 | LCD XP |
| 53 | LCD YP |
| 52 | LCD XM |
| 51 | LCD YM |
| 50 | GPIO PWM1 |
| 49 | LCD BL ON |
| 48 | AUX I2C SCL |
| 47 | AUX I2C SDA |
| 46 | LVDSD0 TX 0 N |
| 45 | LVDSD0 TX 0 P |
| 44 | LVDSD0 TX 1 N |
| 43 | LVDSD0 TX 1 P |
| 42 | LVDSD0 TX 2 N |
| 41 | LVDSD0 TX 2 P |
| 40 | LVDSD0 TX 3 N |
| 39 | LVDSD0 TX 3 P |
| 38 | LVDSD0 CLK N |
| 37 | LVDSD0 CLK P |
| 36 | LVDSD0 TX 0 N |
| 35 | LVDSD0 TX 0 P |
| 34 | LVDSD0 TX 1 N |
| 33 | LVDSD0 TX 1 P |
| 32 | LVDSD0 TX 2 N |
| 31 | LVDSD0 TX 2 P |
| 30 | LVDSD0 TX 3 N |
| 29 | LVDSD0 TX 3 P |
| 28 | LVDSD0 TX 0 N |
| 27 | LVDSD0 TX 0 P |
| 26 | LVDSD0 TX 1 N |
| 25 | LVDSD0 TX 1 P |
| 24 | LVDSD0 TX 2 N |
| 23 | LVDSD0 TX 2 P |
| 22 | LVDSD0 TX 3 N |
| 21 | LVDSD0 TX 3 P |
| 20 | LVDSD0 TX 0 N |
| 19 | LVDSD0 TX 0 P |
| 18 | LVDSD0 TX 1 N |
| 17 | LVDSD0 TX 1 P |
| 16 | LVDSD0 TX 2 N |
| 15 | LVDSD0 TX 2 P |
| 14 | LVDSD0 TX 3 N |
| 13 | LVDSD0 TX 3 P |
| 12 | LVDSD0 TX 0 N |
| 11 | LVDSD0 TX 0 P |
| 10 | LVDSD0 TX 1 N |
| 9 | LVDSD0 TX 1 P |
| 8 | LVDSD0 TX 2 N |
| 7 | LVDSD0 TX 2 P |
| 6 | LVDSD0 TX 3 N |
| 5 | LVDSD0 TX 3 P |
| 4 | LVDSD0 TX 0 N |
| 3 | LVDSD0 TX 0 P |
| 2 | LVDSD0 TX 1 N |
| 1 | LVDSD0 TX 1 P |

REVERSE PINOUT
 however, pin 1 of display connector has reverse convention, so actual footprint is "non-reverse"

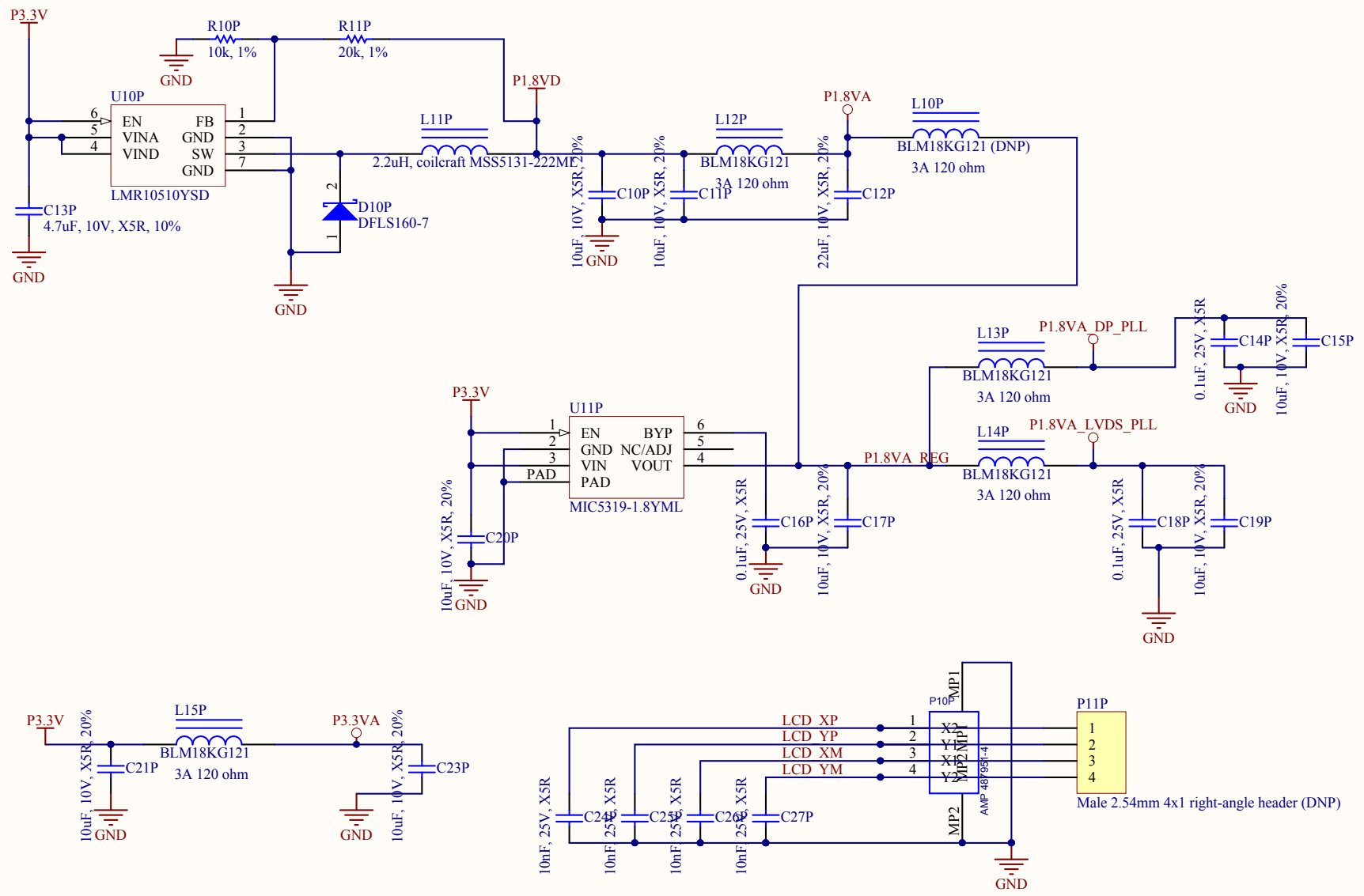


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| Title | | Revision |
|-------|----------------------------------|-----------|
| Size | Number | Revision |
| B | | |
| Date: | 3/27/2014 | Sheet of |
| File: | F:\largework\vit6251_core SchDoc | Drawn By: |

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| | | |
|--------------------------|------------------------------|-----------|
| Title | | |
| LVDS to eDP adapter DVT1 | | |
| Size | Number | Revision |
| A | | |
| Date: | 3/27/2014 | Sheet of |
| File: | F:\largework\...power.SchDoc | Drawn By: |